Serial ATA Supplemental Design Guide

Supplement ID	**005**
Applicable Spec.	**1.0 Gold**

Submission info

Name	Company	Date
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Description of design guidance

This issue was originally identified by Marvell

In order to improve compatibility with some BIOS implementations as well as compensate for slow response from devices in setting the 0x80 value in the Status register upon initialization, host controllers may set the value 0x80 in the Status register upon detecting device presence rather than merely setting the BSY bit (yielding the value0xFF) as defined in the specification.

Supplemental Information

Although the ATA convention is that if the BSY bit in the status register is set the remaining bits are not valid (hence implementations generally add a weak pull-down on the D7 line in order to avoid BSY floating high when no device is present), some BIOS implementations appear to discriminate between the value 0xFF and 0x80 in the Status register during the device presence detection process. When this BIOS behavior is combined with device implementations that are slow to send an initial Register FIS with a status value of 0x80 (indicating it's busy) or which skip this phase entirely and defer until they are ready with a status value ox50 (or similar), a race condition is exposed that may result in the BIOS failing to detect presence of the attached device.

By having the host controller set BSY and clear all other bits in the Status register (yielding the value 0x80) upon determining presence of an attached device (through the PhyRdy indication), instead of merely setting the BSY bit (yielding the value 0xFF), compatibility can be improved for the scenario described above.

Disposition log

1/8/2002	Submitted for review